DIGITAL INDUSTRIES SOFTWARE

The future of semiconductors: Engineering in the convergence era

Reflections from inside an industry undergoing its biggest transformation in decades.

Executive summary
The semiconductor industry is entering a convergence era where silicon, software, physics, packaging, security, AI, and power constraints all intertwine. Device scaling still matters but architecture, integration, verification, and automation will define the industry's trajectory. Organizations that embrace this cross-domain, lifecycle-oriented mindset will define the next decade.

Harry Foster, Chief Scientist Verification, Siemens EDA

Introduction

We're entering a convergence era where silicon, software, physics, packaging, security, AI, and power constraints all intertwine.

Device scaling still matters — but it no longer defines the industry's trajectory. Architecture, integration, verification, and automation do.

And the organizations that embrace this cross-domain, lifecycle-oriented mindset — with verification and agentic AI at the center — will define the next decade.

System-level scaling: Where the real action is

Moore's Law didn't "die." What changed is the economic engine behind it. Transistors still shrink, but the cost-per-transistor advantage that powered decades of predictable scaling is no longer guaranteed.

Today, real breakthroughs come from system-level engineering — from the way we assemble, integrate, and optimize entire platforms:

- Disaggregating designs into chiplet-style components
- Hybrid bonding that pulls memory dramatically closer to compute
- 3DIC techniques (TSVs, wafer-to-wafer stacking, backside power delivery) that extend scaling into the vertical dimension
- HBM and advanced packaging architectures that break bandwidth ceilings
- Photonics to bypass electrical interconnect limits
- Coherency fabrics tying multi-die systems into unified engines

Chiplets still operate mostly within closed internal ecosystems today, but standards like UCIe are finally maturing, and by the end of the decade I expect the first true external chiplet vendors to emerge — limited, curated, but real.

The end of orthogonalization (where it's breaking — and where it still holds)

One of the most underappreciated shifts is the erosion of the clean separation of concerns that defined the 1990s and 2000s.

At the chip level, some of those abstractions still hold. RTL, timing, power, thermals, and software can still be reasoned about with reasonably clean boundaries. But even here, we see erosion:

- Multiple power domains cause power-state–dependent functional behavior
- Thermal gradients shift timing enough to affect correctness
- Mixed-signal blocks blur the digital/analog boundary
- Local workloads influence memory and coherency behavior

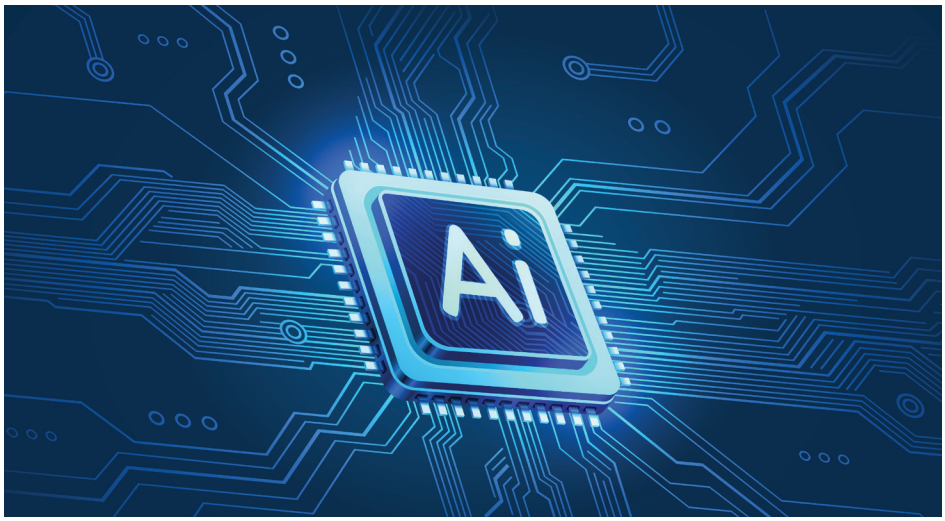
Chip-level orthogonalization isn't gone — but it's no longer airtight.

At the system level, however, orthogonalization has collapsed:

- Hybrid bonding changes timing
- Thermal drift alters latency and coherency
- Photonic bandwidth varies with temperature
- Software load changes physical behavior
- Cross-die interactions emerge between components from different vendors
- In 3DIC stacks, mechanical stress and warpage become functional variables

These aren't packaging footnotes anymore. They are functional behaviors — and that makes them verification challenges.

This shift reflects a broader trend across engineering: electrical, mechanical, physical, and software domains are converging into one integrated system problem. Silicon is simply the first place this convergence is unavoidable.



Digital twins and the new verification model

As boundaries blur, verification must reason across domains that used to be separate:

- logic + physics
- timing + workload
- silicon + software
- multi-die + multi-vendor

This is why digital twins are becoming essential — not the buzzword kind, but the real kind.

A true digital twin is hybrid:

- Simulation for functional accuracy
- Emulation for workload realism
- Prototyping for software development and speed
- Physical solvers for thermals, stress, and electrical effects

No single engine can express system-level truth. Only when these engines converge do we get the fidelity required to understand modern systems.

Software-defined products: When hardware never stops changing

For most of my career, hardware followed a predictable lifecycle: design → verify → tape out → ship → done.

But today:

- AI models evolve monthly
- Security threats emerge weekly
- Workloads shift constantly
- Customer expectations move faster than silicon cycles

To keep up, products have become software-defined. They update firmware, drivers, orchestration layers, and even on-device AI models continuously after deployment.

This flexibility is essential — but it breaks foundational assumptions of verification:

- Correctness is no longer static
- The system in the field diverges from the system validated in the lab
- Failures stem from workload shifts and model drift
- Every over-the-air (OTA) update becomes a verification event

This doesn't eliminate traditional IC verification — it expands it.

Traditional verification + lifecycle verification = the new reality

Verification becomes continuous, not a phase. And digital twins become the bridge that connects design-time assumptions with field-time behavior.

Specialization and domain-specific architectures

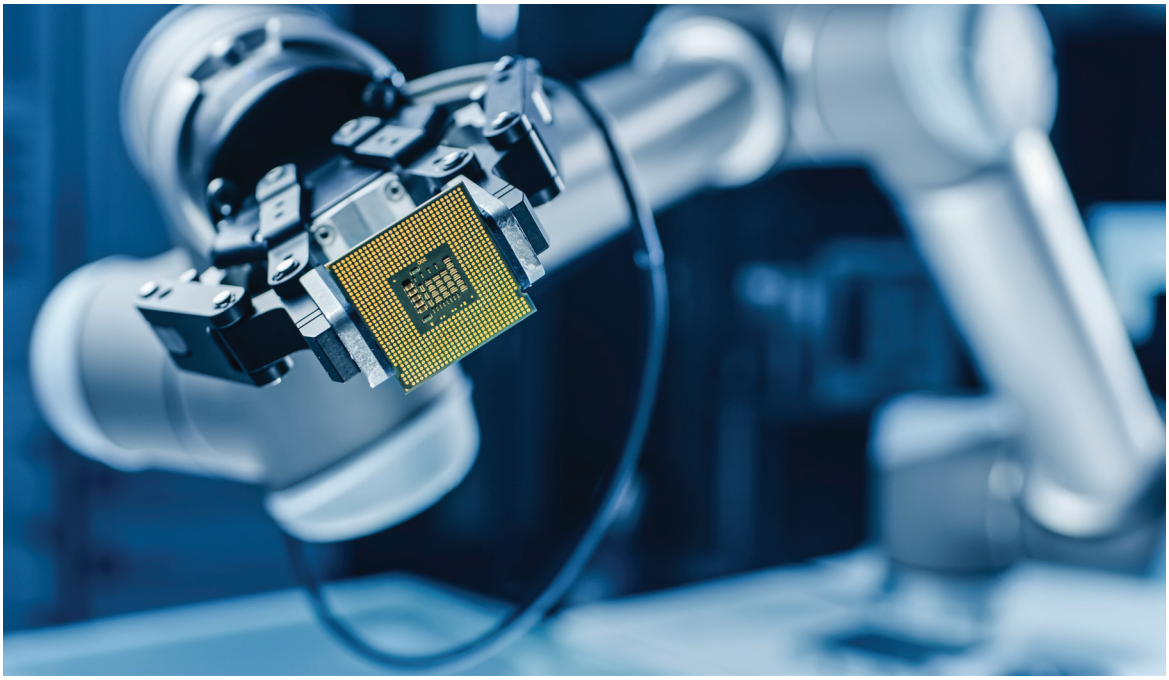
General-purpose scaling has plateaued just as workloads have become more specialized. AI, robotics, graphics, vision, wireless, and real-time control all demand custom or semi-custom architectures.

Domain-specific architectures (DSAs) are no longer niche — they're essential.

But specialization expands verification dramatically:

- Datatype-driven correctness
- Custom ISA extensions
- Reconfigurable dataflows
- Workload-dependent behavior
- Architectures that change as software evolves

Hardware and software now co-evolve, and verification must track that moving boundary.



Memory–compute convergence: The data-movement crisis

The biggest limiter today isn't compute — it's moving data.

To address this, the industry is collapsing the distance between computation and memory:

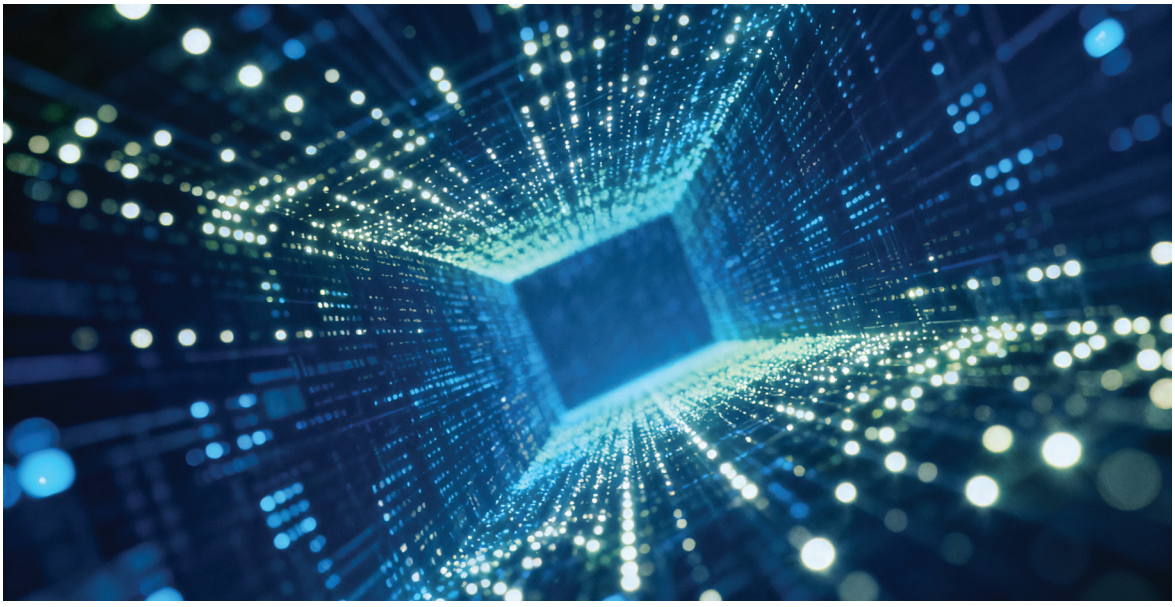
- HBM
- Near-memory compute
- In-memory compute
- Analog accelerators
- Photonics
- Persistent memory layers

But collapsing distance collapses abstraction:

- Thermals change photonic bandwidth
- Analog compute introduces statistical correctness
- Near-memory compute affects ordering
- Cross-die fabrics reshape timing logic
- In 3D stacks, TSV stress modifies electrical behavior

Physics took a multi-decade vacation from digital design — and it's back with a vengeance.

Verification must incorporate these physical and statistical effects.



Security, safety and power: Now architectural

Chiplets shift trust boundaries.

OTA updates expand attack surfaces.

AI models drift unpredictably.

Security and safety aren't procedural anymore — they are architectural verification domains.

Power has also become a first-class constraint:

- Data centers hit regional limits
- AI training burns megawatts
- Verification infrastructure consumes massive compute

Capability isn't the limit — energy is.

Verification strategies must integrate power-aware planning, regression optimization, and lifecycle energy modeling.

Agentic AI: The workflow copilot (a transformative shift)

AI already enhances individual verification tools. But the next leap — and perhaps the most disruptive — is agentic AI orchestrating entire verification workflows.

This is not "AI as a feature." This is AI as the conductor of the entire verification process.

Agentic AI will:

- Interpret verification intent
- Plan and schedule verification engines
- Generate and refine constraints
- Analyze regressions and root-cause failures
- Maintain consistency across simulation, emulation, and prototyping
- Retarget verification after OTA updates
- Manage compute and power budgets
- Coordinate hybrid digital twins

In other words: Engineers provide intent; agentic AI handles iteration depth.

Given the complexity, dynamism, and multidisciplinary nature of modern systems, agentic AI will become foundational — not optional — to verification productivity. Unified environments such as Questa One are deliberately evolving to provide the substrate agentic AI will orchestrate across.

Engineering in the convergence era

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