Siemens EDA Xcelerator Academy

Guide Your Learning Journey With @oneGlance Maps

Use the maps as visual guides of the recommended flow of learning. Each course entry shows available method of delivery and is linked to course datasheets and sign-up requests.

Systems Design and Manufacturing
Xpedition | HyperLynx | PADS Standard | PADS Professional | Valor NPI

Hardware Assisted Verification
Veloce

High-level Synthesis and Verification
Catapult | Vista

IC Analog/Mixed Signal Verification
Eldo | Questa ADMS | AFS | A/MS HDLs | Symphony

Power Analysis and Optimization
PowerPro

IC Design, Verification and Implementation
Tanner EDA | Calibre | Aprisa

IC Design, Manufacturing, and Test
Tessent | Tessent Embedded Analytics

IC Logic Design
HDL Designer | ReqTracer | Design Language | Questa Lint

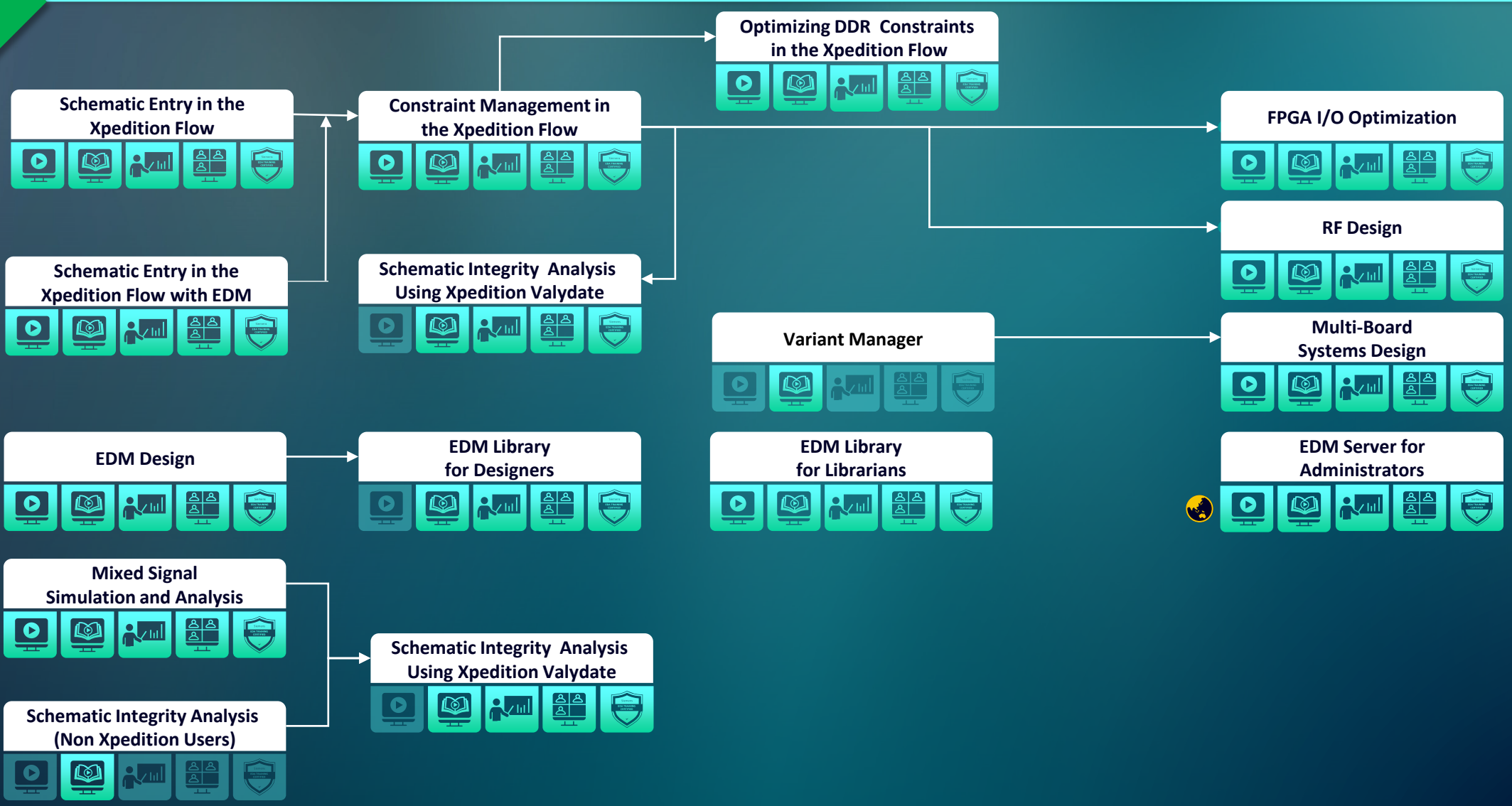
IC Logic Verification
Language and Methodology | Functional Safety | Verification Tools

IC Packaging
Xpedition ICP

SIEMENS
@oneGlance

ELECTRONIC SYSTEMS DESIGN & MFG
XPEDITION LEARNING PATHS 1 of 2

INTRODUCTION | INTERMEDIATE | MASTERY



Schematic Entry | EDM | Schematic Analysis

Self-paced Course | Self-paced Library | Instructor -led Training | Remote Instructor-led | Badging/ Certification | Localization Available

SIEMENS @oneGlance

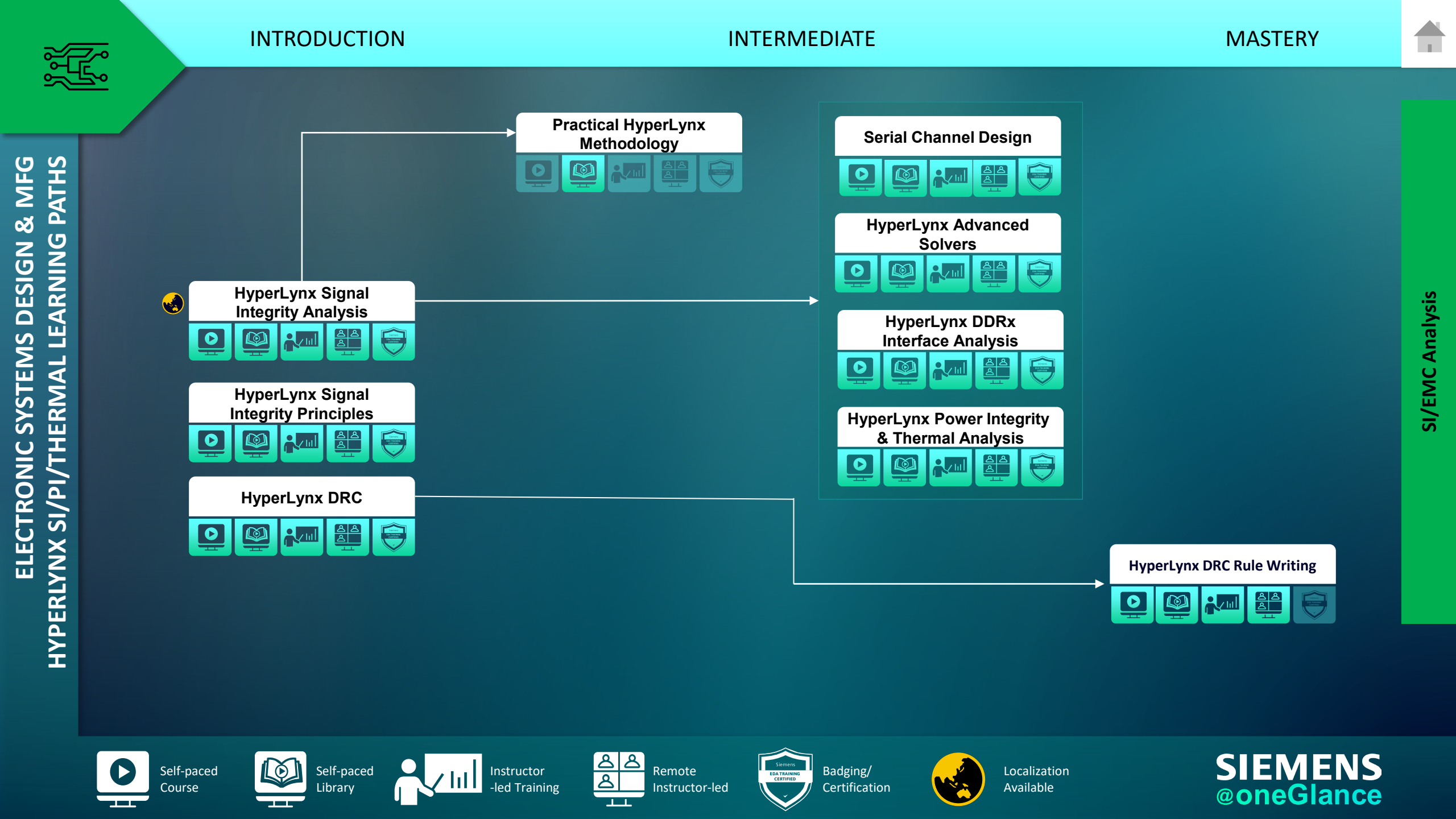
ELECTRONIC SYSTEMS DESIGN & MFG
XPEDITION LEARNING PATHS 2 of 2

INTRODUCTION | INTERMEDIATE | MASTERY

PCB Layout | Lib Mgmt. | Valor NPI

Self-paced Course | Self-paced Library | Instructor -led Training | Remote Instructor-led | Badging/ Certification | Localization Available

SIEMENS @oneGlance


INTRODUCTION
INTERMEDIATE
MASTERY
ELECTRONIC SYSTEMS DESIGN & MFG
HYPERLYNX SI/PI/THERMAL LEARNING PATHS
Practical HyperLynx Methodology
HyperLynx Signal Integrity Analysis
HyperLynx Signal Integrity Principles
HyperLynx DRC
Serial Channel Design
HyperLynx Advanced Solvers
HyperLynx DDRx Interface Analysis
HyperLynx Power Integrity & Thermal Analysis
HyperLynx DRC Rule Writing
SI/EMC Analysis
Self-paced Course
Self-paced Library
Instructor -led Training
Remote Instructor-led
Badging/ Certification
Localization Available
SIEMENS
@oneGlance

PRODUCT EXPLORATION
HYPERLYNX: HIGH-SPEED DESING ANALYSIS

Explore HyperLynx

5 | 22 | 83 | 5

A complete family of analysis tools for high-speed electronic design including DDR, DRC, DC, Signal, Power Integrity, 3D and more. To access this library for free, enter promotional code ExploreVEP__30 in the shopping cart to register.

1. A Journey Through HyperLynx
2. Workshop: Post-layout PCIe Gen3 Compliance Verification
6. Workshop: Compliance-based Serial Link Design and Verification
4. Workshop: DDR5 Model-free Post-layout Verification
2. Workshop: DDR4-Focused DRC

3. Workshop: Design Space Exploration(DSE): Differential Via Optimization
4. Workshop: DDR4 Power Aware
2. Workshop: DC Drop

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance

ELECTRONIC SYSTEMS DESIGN & MFG
PADS STANDARD/PLUS LEARNING PATHS

INTRODUCTION | INTERMEDIATE | MASTERY

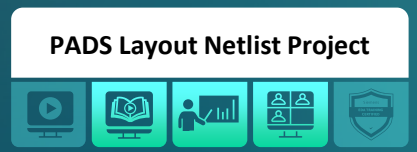
Getting Started with PADS Standard Plus

Schematic Entry in PADS Integrated Flow

Schematic Entry in PADS Netlist Flow

PADS Layout for an Integrated Project

PADS Layout Netlist Project



Library Management in PADS Integrated Flow

Library Management in PADS Netlist Flow

Schematic

PCB Layout

Library Mgmt.

Self-paced Course

Self-paced Library

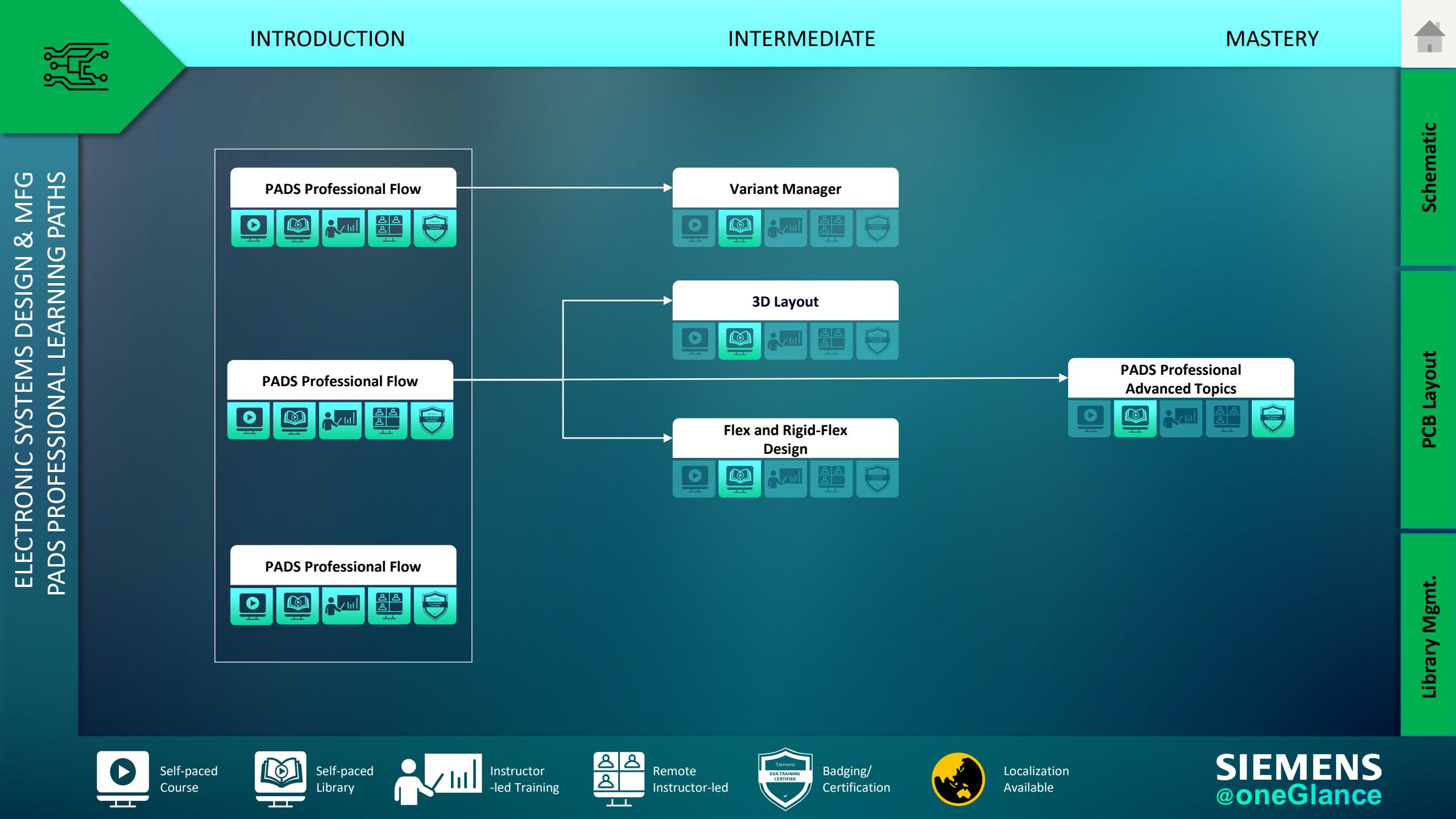
Instructor -led Training

Remote Instructor-led

Badging/ Certification

Localization Available

SIEMENS @oneGlance


INTRODUCTION
INTERMEDIATE
MASTERY
ELECTRONIC SYSTEMS DESIGN & MFG
PADS PROFESSIONAL LEARNING PATHS
PADS Professional Flow
PADS Professional Flow
PADS Professional Flow
Variant Manager
3D Layout
Flex and Rigid-Flex Design
PADS Professional Advanced Topics
Schematic
PCB Layout
Library Mgmt.
Self-paced Course
Self-paced Library
Instructor -led Training
Remote Instructor-led
Badging/ Certification
Localization Available
SIEMENS
@oneGlance

EMULATION & PROTOTYPING LEARNING PATHS

INTRODUCTION | INTERMEDIATE | MASTERY

Emulation

Veloce Basic → **Advanced Topics for Emulation using Veloce** → **Veloce Solutions**

Prototyping

Veloce proFPGA Basic

Veloce Primo Basic

Self-paced Course

Self-paced Library

Instructor -led Training

Remote Instructor-led

Badging/ Certification

Localization Available

SIEMENS @oneGlance

INTRODUCTION | INTERMEDIATE | MASTERY

HIGH LEVEL SYNTHESIS LEARNING PATHS

Catapult Basic C++ & High-level Synthesis

Design & Verification w/ System C & MatchLib

Catapult High-Level Verification

Introduction to Vista

High-level Synthesis & Verification

Architectural Design & Exploration

Self-paced Course

Self-paced Library

Instructor -led Training

Remote Instructor-led

Badging/ Certification

Localization Available

SIEMENS @oneGlance

PRODUCT EXPLORATION
Catapult: High-level Synthesis and Verification

Explore Catapult

5 | 37 | 144 | 7

Description

The Catapult High-Level Synthesis (HLS) library contains a set of modules to introduce Engineers to HLS and High-Level Verification. To access this library for free, click any of the boxes on this page and use promotional code ExploreVEP__30 in the shopping cart.

1	Learning Center Overview and Catapult Curriculum
6	Design and Verification Using SystemC and MatchLib
16	Catapult Basic C++ and High-level Synthesis
8	Catapult High-level Verification
1	Catapult basic C++ and High-Level Synthesis Exam

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance

PRODUCT EXPLORATION
PowerPro: Power Analysis & Optimization

Explore PowerPro

3 | 7 | 66 | 3

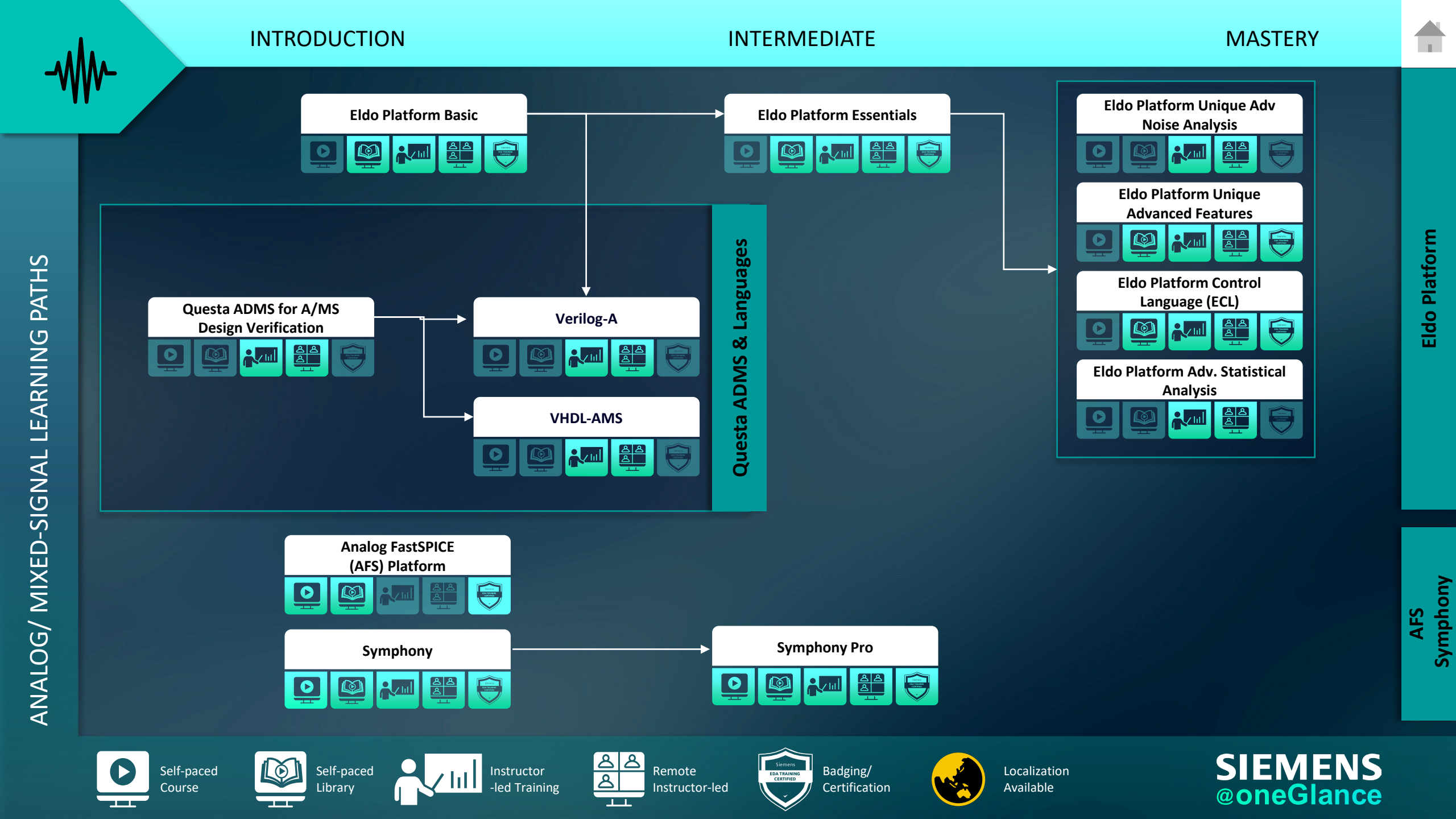
- 3 — PowerPro One-on-One
- 2 — PowerPro Power Analysis
- 2 — RTL Power Optimization

Description

Learn how to use PowerPro for power analysis/estimation at both RTL and gate-level and how to optimize power during RTL development for the lowest possible design power. To access this library for free, enter promotional code ExploreVEP__30 in the shopping cart to register.

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance


INTRODUCTION
INTERMEDIATE
MASTERY
ANALOG/ MIXED-SIGNAL LEARNING PATHS
Eldo Platform Basic
Eldo Platform Essentials
Eldo Platform Unique Adv Noise Analysis
Eldo Platform Unique Advanced Features
Eldo Platform Control Language (ECL)
Eldo Platform Adv. Statistical Analysis
Eldo Platform
Questa ADMS for A/MS Design Verification
Verilog-A
VHDL-AMS
Questa ADMS & Languages
Analog FastSPICE (AFS) Platform
Symphony
Symphony Pro
AFS Symphony
Self-paced Course
Self-paced Library
Instructor -led Training
Remote Instructor-led
Badging/ Certification
Localization Available
SIEMENS
@oneGlance

PRODUCT EXPLORATION
AMS Verification

Explore AMS Verification

2 | 2 | 9 | 2

- 1 **Circuit Simulation**
- 1 **Mixed-signal**

Description

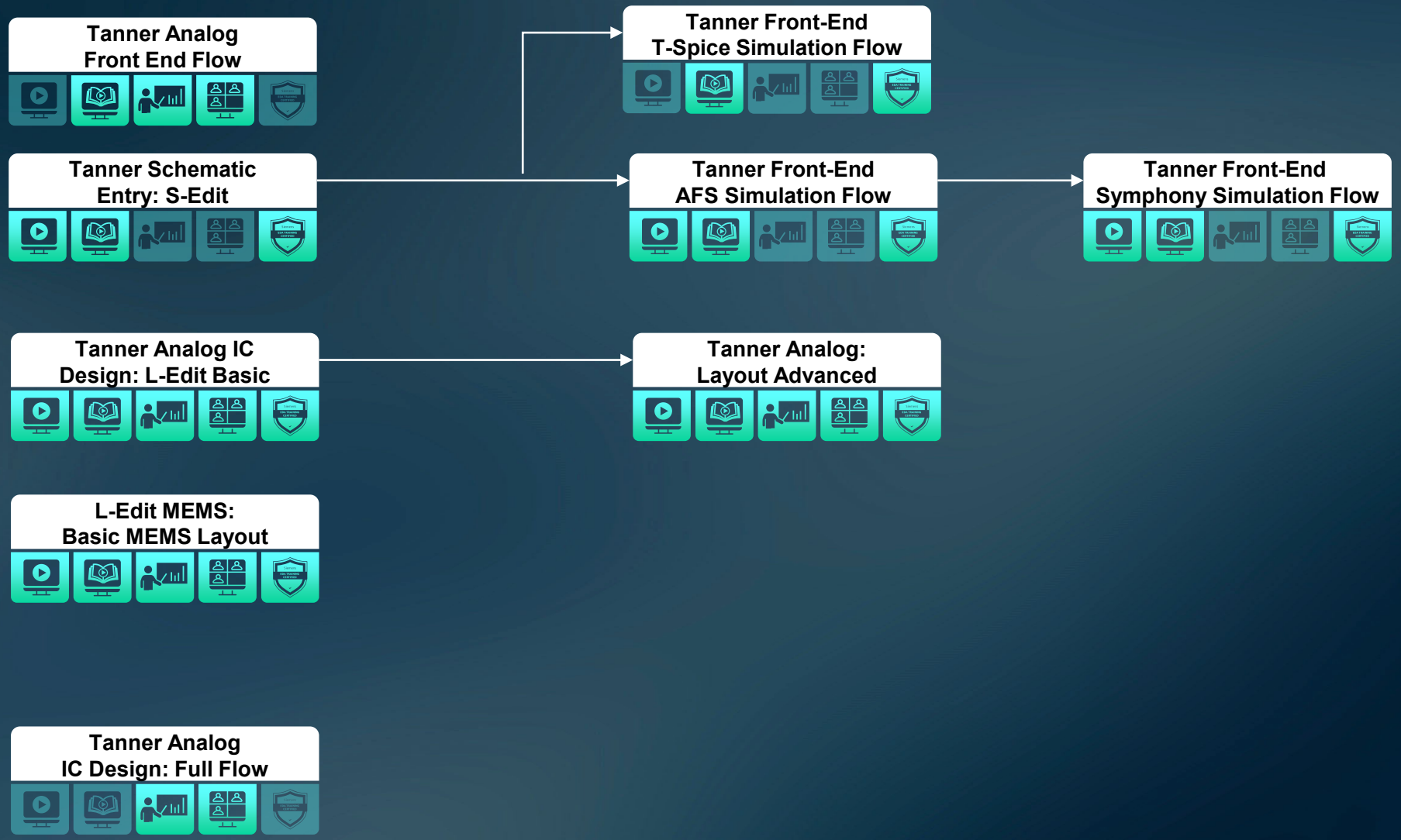
Explore Siemens Analog Mixed-Signal Verification Solutions – consistently delivering proven and differentiated capabilities to 1000+ customers worldwide. To access this library for free, click buy and enter promotional code **ExploreVEP__30** in the shopping cart.

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance

TANNER EDA LEARNING PATHS

INTRODUCTION | INTERMEDIATE | MASTERY



Design Creation & Simulation (Front-End)

Design Layout (Back-End Flow)

Full IC Flow

Self-paced Course

Self-paced Library

Instructor -led Training

Remote Instructor-led

Badging/ Certification

Localization Available

SIEMENS @oneGlance

PRODUCT EXPLORATION

Siemens Analog/Mixed Signal Custom Design Flow

Explore AMS IC Design

5 | 10 | 30 | 3

Description

Explore Siemens custom analog IC design flow to increase productivity from design capture, simulation, physical layout, and verification to tape-out. To access this library for free, enter promotional code **ExploreVEP__30** in the shopping cart to register.

1. The Full Flow Overview
2. Schematic Capture and Simulation
4. Physical Layout and Verification
2. Foundry Reference Flows
1. The Library Manager

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance

CALIBRE LEARNING PATHS

1 of 3

INTRODUCTION

INTERMEDIATE

MASTERY

Using Calibre nmDRC/nmLVS

Using DESIGNrev

Writing Calibre nmDRC/nmLVS Rules

Using PERC/Working with PERC

Calibre xRC Parasitic Extraction

Calibre xACT/xACT 3D

Tcl/Tk for Calibre Applications

Calibre TVF

Comp. Calibre PERC Coding/Writing PERC Rules

nmLVS Debug Case Studies

Calibre Pattern Matching

IC Verification Engineer

Using Calibre nmDRC/nmLVS

Using DESIGNrev

Calibre Multi-Patterning

Tcl/Tk for Calibre Applications

DESIGNrev Scripting

IC Layout Engineer


Self-paced Course


Self-paced Library


Instructor -led Training


Remote Instructor-led

Badging/ Certification


Localization Available

SIEMENS
@oneGlance

CALIBRE LEARNING PATHS

2 of 3

INTRODUCTION	INTERMEDIATE	MASTERY

CAD Engineer

- Using Calibre nmDRC/nmLVS
- Writing Calibre nmDRC/nmLVS Rules
- Calibre xRC Parasitic Extraction
- Calibre xACT/xACT 3D
- Using PERC/Working with PERC
- Mastering Calibre eqDRC
- Calibre TVF
- Comp. Calibre PERC Coding/Writing PERC Rules

Circuit Designer

- Using DESIGNrev
- DESIGNrev Scripting
- Tcl/Tk for Calibre Applications
- Using PERC/Working with PERC
- Comp. Calibre PERC Coding/Writing PERC Rules

Self-paced Course

Self-paced Library

Instructor -led Training

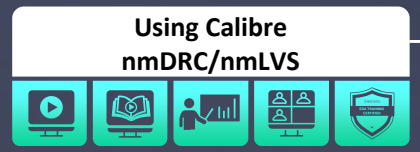
Remote Instructor-led

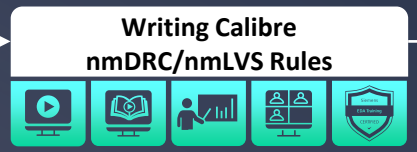
Badging/ Certification

Localization Available

SIEMENS @oneGlance

CALIBRE/ APRISA LEARNING PATHS





Foundry Engineer

Physical Implementation Engineer

Self-paced Course

Self-paced Library

Instructor -led Training

Remote Instructor-led

Badging/ Certification

Localization Available

SIEMENS @oneGlance

PRODUCT EXPLORATION
Calibre IC Design and Verification

Explore Calibre

6 | 12 | 79 | 6

Description

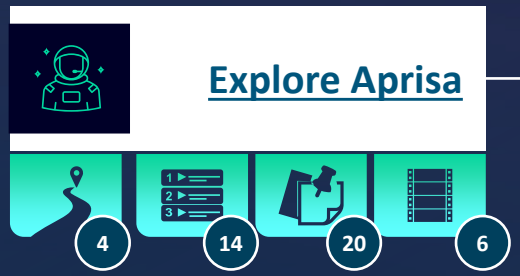
Discover the industry-leading Calibre tool suite capabilities and how this content can solve your day-to-day common IC design problems, including circuit reliability problems, analog layout issues, and other common design challenges. To access this library for free, click buy and enter promotional code **ExploreVEP__30** in the shopping cart.

- 1 — User Experience
- 2 — Advanced Customer Experience - Calibre PERC
- 1 — Advanced Customer Experience in Japanese
- 1 — Calibre mPower EM/IR
- 6 — New Customer Experience - Product Overviews and How-to-Get Started Guides
- 1 — Advanced Customer Experience - How to Accelerate Faster Time to Closure Using Calibre Capabilities

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance

PRODUCT EXPLORATION
Aprisa



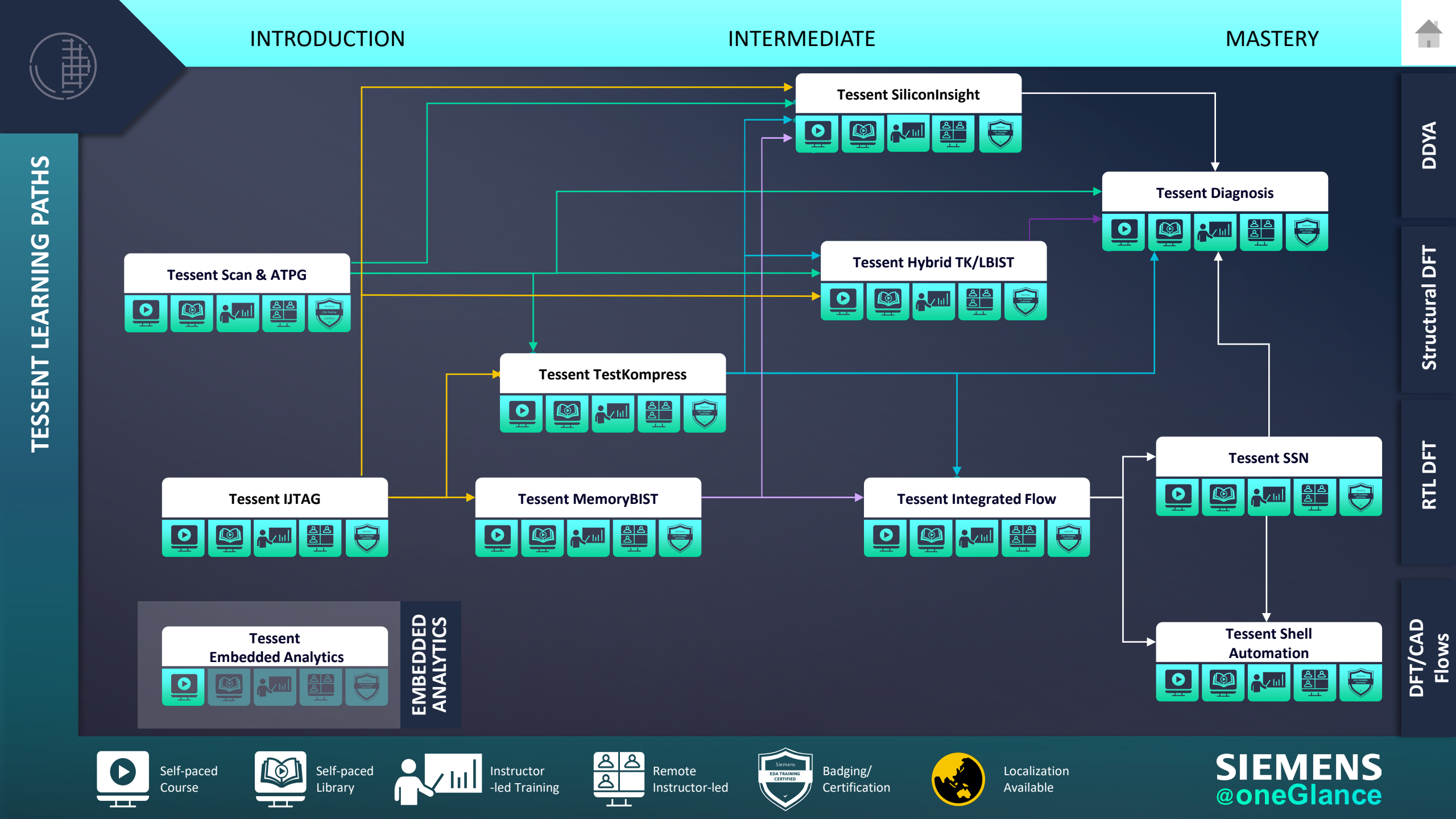
Description

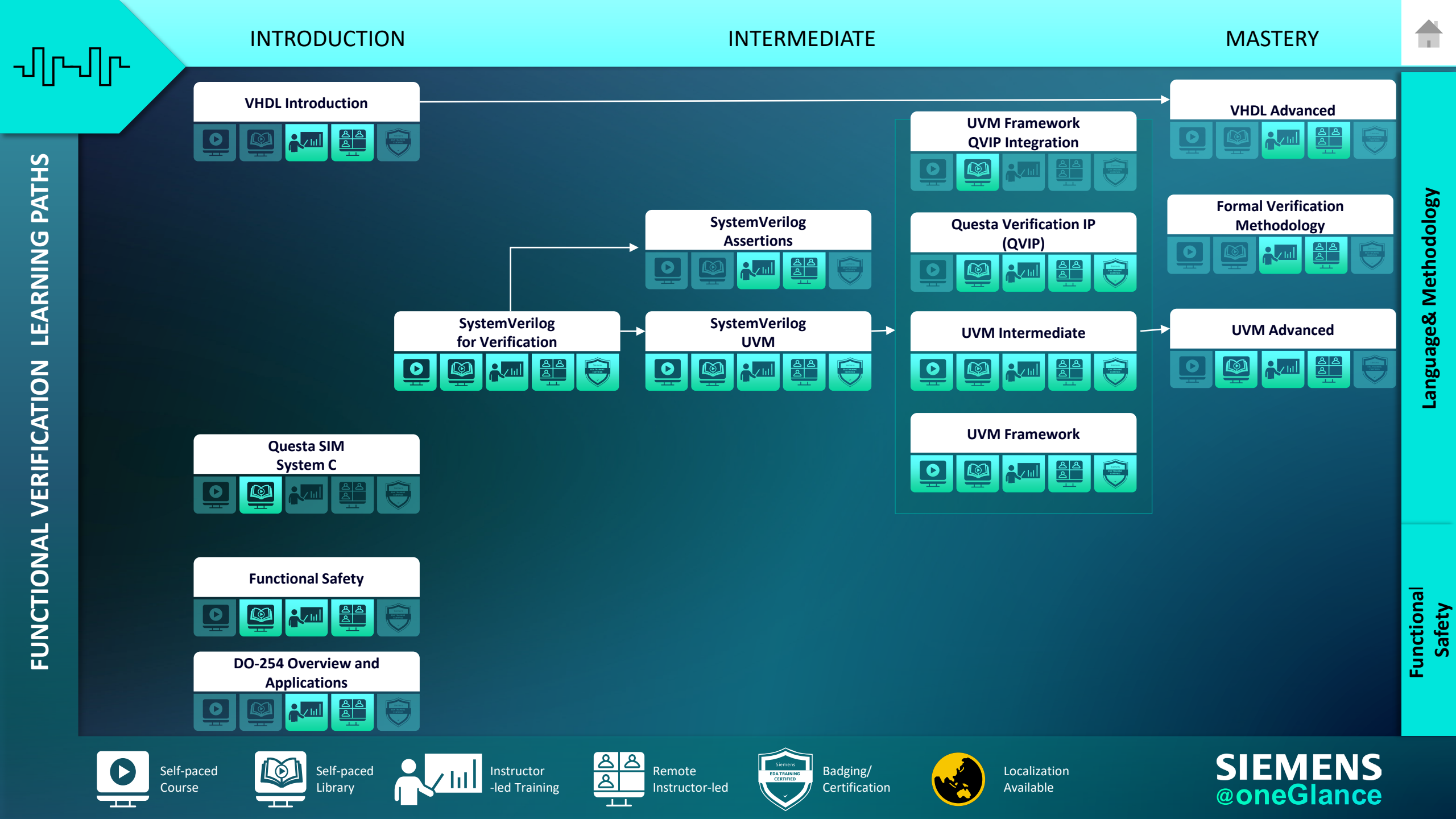
Explore Siemens Place and route technology for top-level and block-level implementation of complex SoC designs. Find out how the detail-route-centric architecture and hierarchical database can enable you to achieve fast design closure with optimal quality of results. To access this library for free, click buy and enter promotional code **ExploreVEP__30** in the shopping cart.

- 1 — Aprisa Webinars
- 1 — Getting Started with Aprisa
- 11 — Aprisa Basic Training
- 1 — Aprisa Techforum 2023

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance


INTRODUCTION
INTERMEDIATE
MASTERY
TESSENT LEARNING PATHS
Tessent SiliconInsight
Tessent Diagnosis
Tessent Scan & ATPG
Tessent Hybrid TK/LBIST
Tessent TestKompress
Tessent IJTAG
Tessent MemoryBIST
Tessent Integrated Flow
Tessent SSN
Tessent Shell Automation
Tessent Embedded Analytics
EMBEDDED ANALYTICS
DDYA
Structural DFT
RTL DFT
DFT/CAD Flows
Self-paced Course
Self-paced Library
Instructor -led Training
Remote Instructor-led
Badging/ Certification
Localization Available
SIEMENS
@oneGlance


INTRODUCTION
INTERMEDIATE
MASTERY
FUNCTIONAL VERIFICATION LEARNING PATHS
VHDL Introduction
VHDL Advanced
UVM Framework
QVIP Integration
SystemVerilog
Assertions
Questa Verification IP
(QVIP)
Formal Verification
Methodology
SystemVerilog
for Verification
SystemVerilog
UVM
UVM Intermediate
UVM Advanced
Questa SIM
System C
UVM Framework
Functional Safety
DO-254 Overview and
Applications
Language& Methodology
Functional
Safety
Self-paced
Course
Self-paced
Library
Instructor
-led Training
Remote
Instructor-led
Badging/
Certification
Localization
Available
SIEMENS
@oneGlance

FUNCTIONAL VERIFICATION & DESIGN CREATION LEARNING PATHS

INTRODUCTION | INTERMEDIATE | MASTERY

Verification Tools

- Questa Core HDL Simulation → ModelSim/Questa Core Advanced Topics → Mastering Questa
- Visualizer Debug Environment → Visualizer Advanced
- Questa Formal Verification
- FPGA Equivalency Checking
- Questa Clock Domain Crossing Verification
- Questa Power Aware and UPF
- Questa SIM System C

Design Creation

- HDL Designer Series
- ReqTracer for FPGA/ ASIC Design Assurance
- SystemVerilog for Design
- Questa Lint

Self-paced Course | Self-paced Library | Instructor -led Training | Remote Instructor-led | Badging/ Certification | Localization Available

SIEMENS @oneGlance

PRODUCT EXPLORATION
Questa Functional Verification

Explore Questa Functional Verification

8 | 8 | 38 | 5

Description

Discover Questa prime's advanced verification capabilities To access this library for free, click buy and enter promotional code **ExploreVEP__30** in the shopping cart.

- 1 Code Coverage
- 1 UVM Testbench Generation
- 1 Functional Coverage
- 1 Questa Clock Domain Crossing
- 1 Visualizer Coverage Debug
- 1 UPF and Questa Power Aware
- 1 Advanced Verification for Verilog and VHDL
- 1 Introduction to UVVM

Learning Paths | # of Chapters | # of Topics | Hours of video

SIEMENS @oneGlance

XPEDITION IC PACKAGING SOLUTIONS LEARNING PATHS

Package Design

Self-paced Course
Self-paced Library
Instructor -led Training
Remote Instructor-led
Badging/ Certification
Localization Available

SIEMENS @oneGlance